CLAIMS

What is claimed is:

1. A method comprising:

fixing a logical identifier for a signal line at an egress interface;

mapping a first physical identifier for a first physical signal line to the logical identifier; and

remapping a second physical identifier for a second physical signal line to the logical identifier responsive to a line failure on the first physical signal line.

2. The method of claim 1 wherein mapping comprises:

writing to a cross connect table and wherein remapping comprises rewriting the cross connect table.

3. The method of claim 1 further comprising:

switching a signal from a second physical signal line to a physical line corresponding to the logical identifier responsive to the remapping.

4. The method of claim 1 wherein fixing comprises:

assigning an identifier to each port of the egress interface during initialization; and

preventing change to the identifier after initialization.

5. The method of claim 1 wherein the signal line is a synchronous optical networking (SONET) line.

6. An apparatus comprising:

a bus interface;

an ingress time slot interchange (ITSI) module;

a switch fabric coupled to the ITSI module;

an egress time slot interchange (ETSI) module having a plurality of inputs, each input assigned a logical identifier which remains fixed after initialization; and

a translation module to translate an incoming signal identifier to one of the logical identifiers independent of a physical line on which the signal is received.

7. The apparatus of claim 6 wherein the translation module comprises:
a cross connect table.

8. The apparatus of claim 1 further comprising:
a bus coupled to the bus interface;
a termination module coupled to the bus; and
a line interface having an optical to electrical (O/E) and electrical to optical (E/O) converter.

9. The apparatus of claim 6 wherein the apparatus is implemented as an ASIC on a backplane of a line card.